The University of Texas Rio Grande Valley
College of Engineering and Computer Science
Department of Electrical & Computer Engineering

EECE 3302.01 Electronics 2
Spring 2025

Electronics Lab Report
2 Stage CMOS Op Amp Build and Test

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May 12, 2025

Contents

I. ABSTRACT

A two-stage CMOS operational amplifier (op amp) was designed, built, and tested using ALD MOSFET quad arrays (ALD1105, ALD1106, and ALD1107) with dual ±3V power supplies. The experimental tests conducted included verifying transistor saturation, measuring open-loop comparator behavior, step response, slew rates, frequency response, voltage swing, and gain-bandwidth product. The measured current source achieved ~70.1 μA, with an initial power dissipation of 0.3893 mW. Open-loop testing validated the circuit's comparator functionality with clearly distinguishable inverted and non-inverted outputs. The compensated amplifier exhibited a step response settling time of 4.4 μs, rising edge slew rate of 9.31 V/μs, falling edge slew rate of 0.660 V/μs, and a gain-bandwidth product of 1.64 MHz with a voltage swing of 4.24 V peak-to-peak.

II. BODY

For Electronics 2 Project, it was asked to build a 2 Stage CMOS Op Amp and test it by using +/- 3V power supplies and ALD MOSFET quad arrays which means that in each chip, there are four MOSFET transistors made on the same substrate which is important when building amplifiers. The parts that were used were the following: ALD1106, ALD1107, and ALD1105 chips with the circuit schematic that was given displayed below which was used to implement it onto a breadboard.

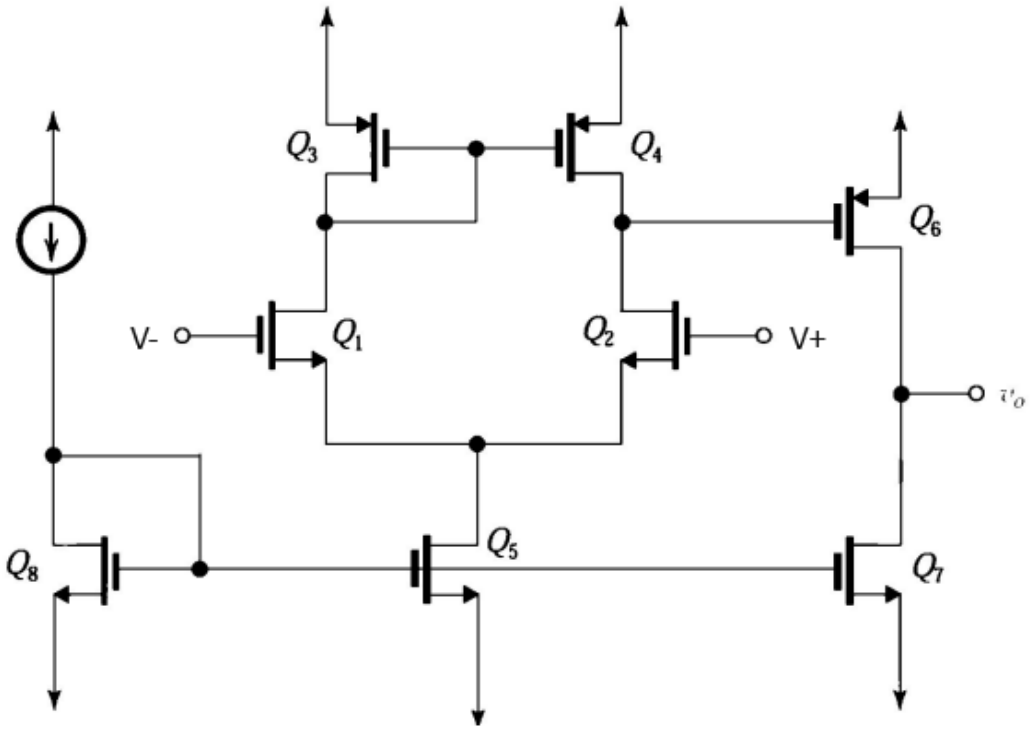


Figure 1 - Circuit Schematic Used to Build 2 Stage CMOS Op Amp

It was also recommended by the instructor to double up some of the transistors for the circuit to work as intended, by "doubling up" it essentially means making them bigger by putting the transistors in parallel; in order to do that, each terminal will be connected for example, drain

to drain, gate to gate, and source to source to double them up which the following transistors needed to be doubled up per chip as recommended by instructor:

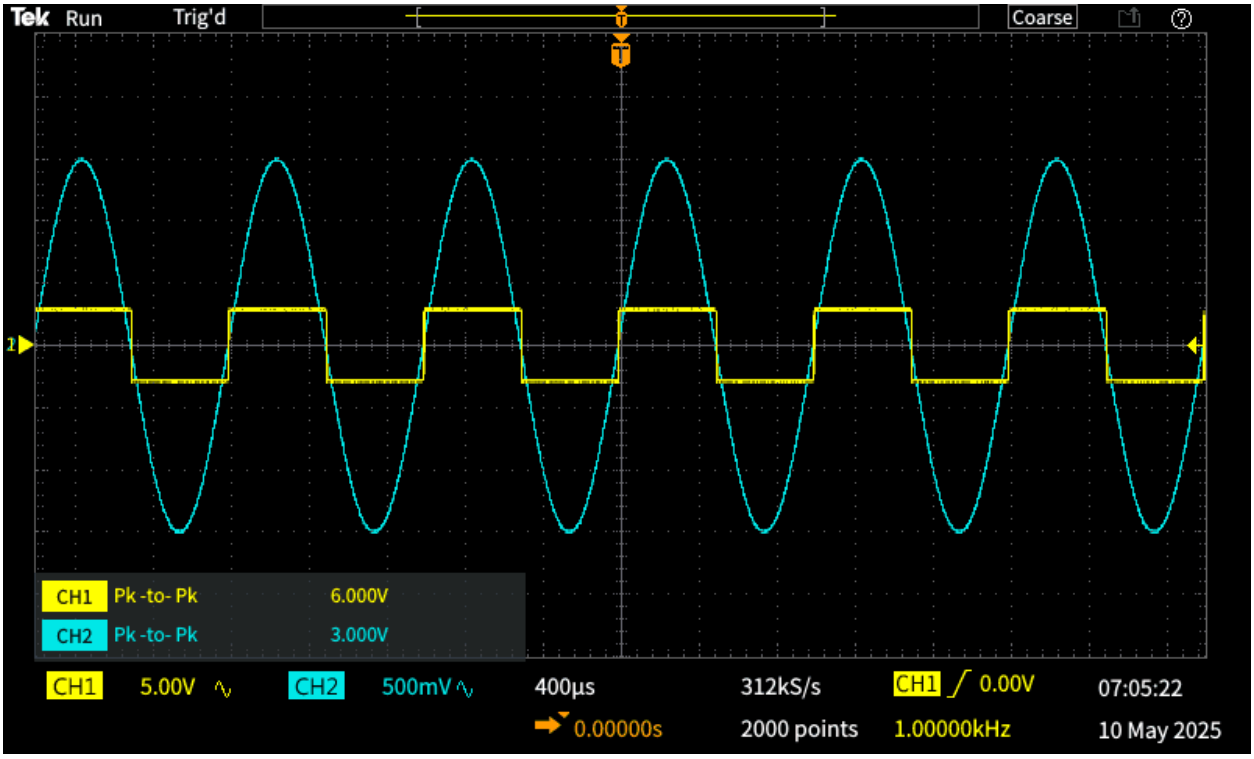
- ALD1106: 2XQ5, Q7 and Q8
- ALD1107: 2XQ3 and 2XQ4
- ALD1105: Q1, Q1 and 2XQ6

PART 1: INITIAL BUILD AND TEST

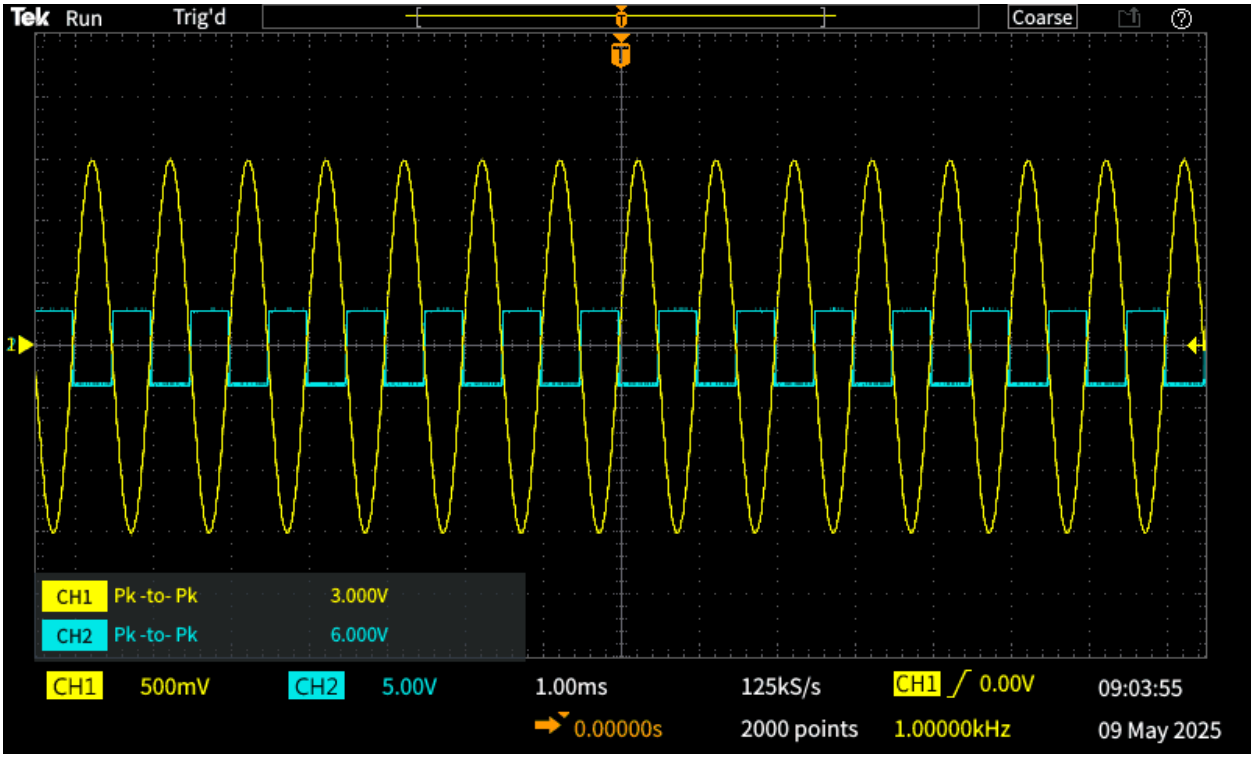
After doubling up the transistors, a current source needed to be implemented in the circuit which goes into the drain terminal of the Q8 NMOS transistor. The current had to be picked which we picked a current of 75 µA as it was recommended to pick a current between 50 – 100 µA. The way that current source of 75 µA was implemented was by using Ohm's law of R = V/I and knowing that we're using the positive 3V rail we can do the following R = 3V/75 µA = 40kΩ. The current from the power supply was limited to 0.001 A or 1 mA so that nothing burns if connections were wrongly placed and the measured current ended up being around ~70.1 uA.

For part 1.3 it was asked to calculate power dissipation for the entire circuit with both inputs grounded, the way we did it was by calculating the power that was being thrown into the circuit minus the power that is being used by the circuit. For example, the power of the power supply is 6 mW because it's a dual power supply with the positive channel using 3V and 0.001 A which is 3 mW, then the negative rail using 3V and 0.001 A totaling 6 mW, then measuring the total voltage and current being used on the circuit it was calculated to be 6.3893 mW so subtracting both the power dissipated ended up being 0.3893 mW.

For part 1.4 it was asked to input a 1 kHz sine wave with an amplitude of VDD/2 which is 3V/2 = 1.5V amplitude into the non-inverting terminal while grounding the inverting terminal and observing the output at "v_o" and then inputting that sine wave into the inverting terminal and grounding the non-inverting terminal and observe the output "v_o" with the oscilloscope. The circuit should act like a comparator meaning that the output should be a square wave, the following scope shots are of the non-inverted output and inverted output:



Scope Shot 1 - Non-Inverted Output with Sine Wave Going Into V+ and V- Grounded

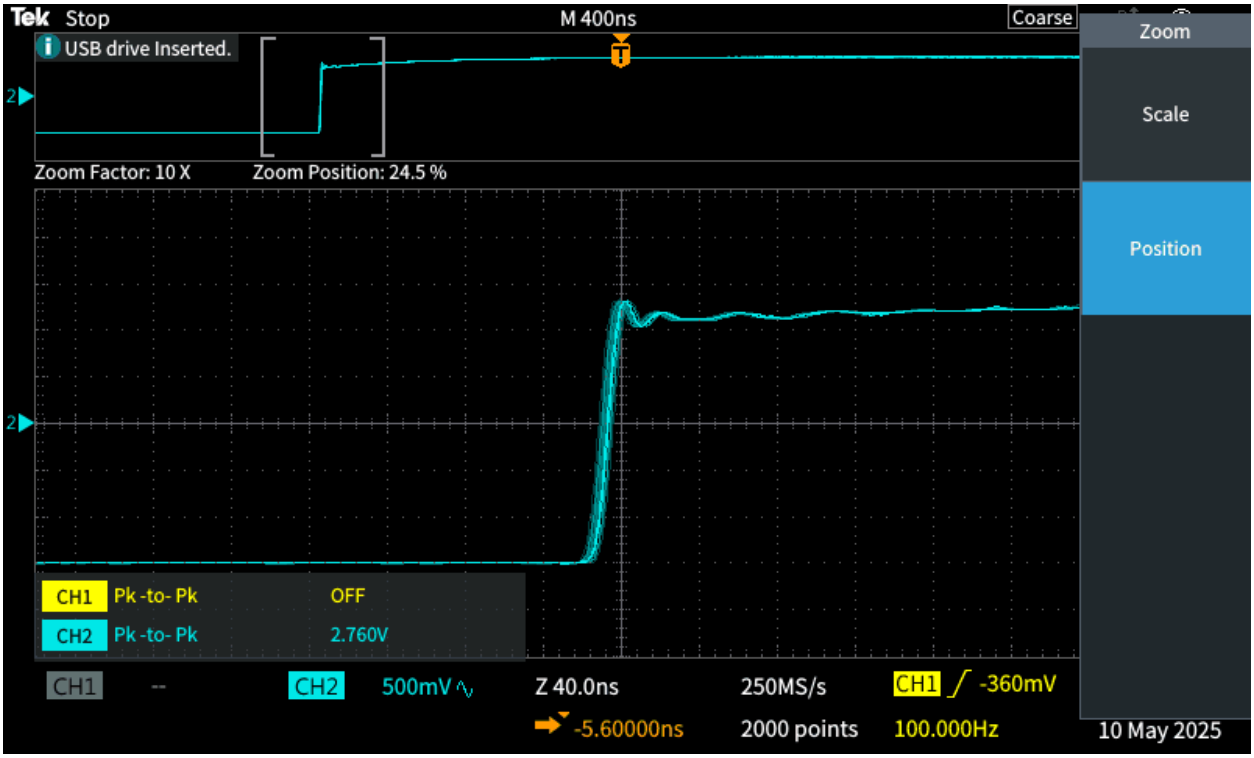


Scope Shot 2 - Inverted Output with Sine Wave Going Into V- and V+ Grounded

PART 2: COMPENSATION

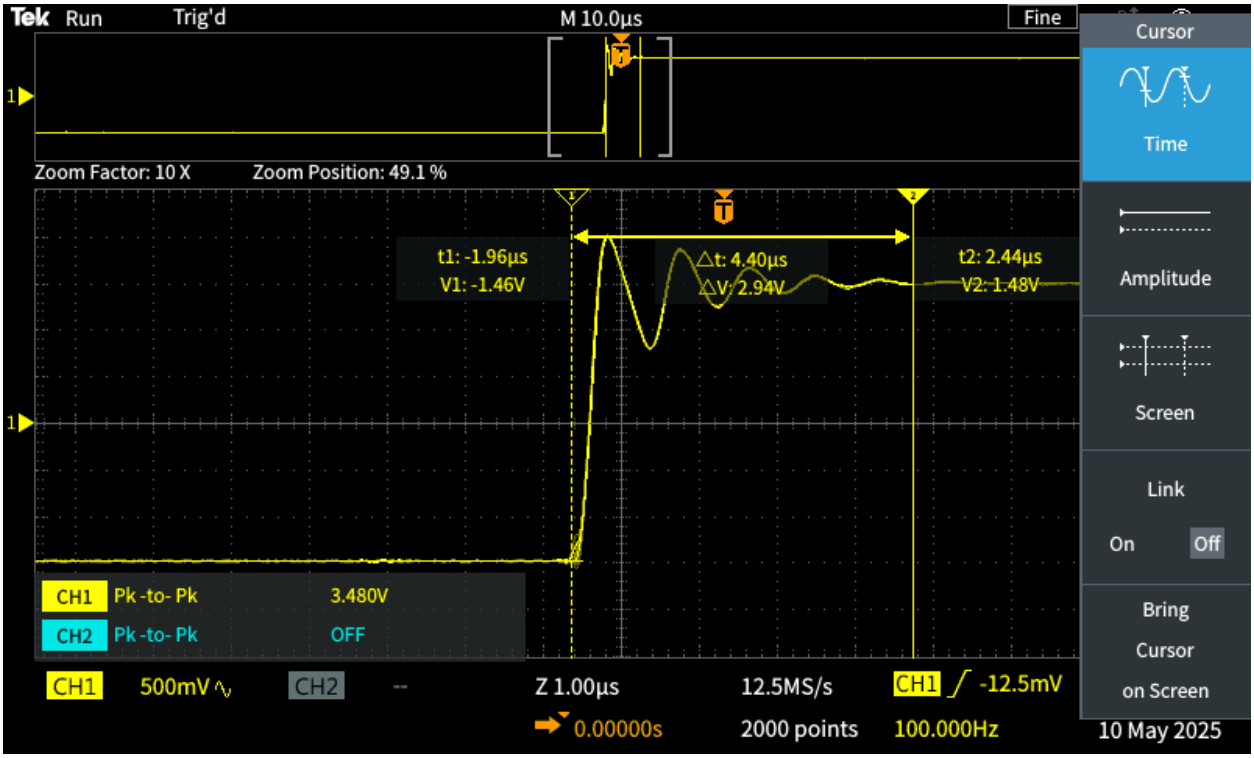
For part 2 of Electronics 2 Project, it is asked to wire the op amp as a voltage follower which means that the V- terminal from the op amp will be directly connected to the output of the 2 Stage Amplifier to have negative feedback making it a voltage follower which means that whatever waveform it is inputted, it is also outputted. It also asked to connect the compensation capacitor (C_C) and variable resistance (R) using a potentiometer between the input and output terminals of the common source stage. A compensation capacitor of 100 pF and a 5k Ω potentiometer was used to vary the resistance to get the sharpest edges. The way to do that would be to input a 100 Hz square wave with zero offset and an amplitude of VDD/2 = 3V/2 = 1.5V amplitude and by using the "Zoom" function on the oscilloscope it lets us see the rising edge

very clearly so we can adjust the compensation capacitor and vary the resistance to get a good step response which is not over damped or under damped but in between. Which the following scope show includes the step response of the circuit by varying the compensation capacitor and resistance using the potentiometer:



Scope Shot 3 - Step Response of the Voltage Follower Circuit

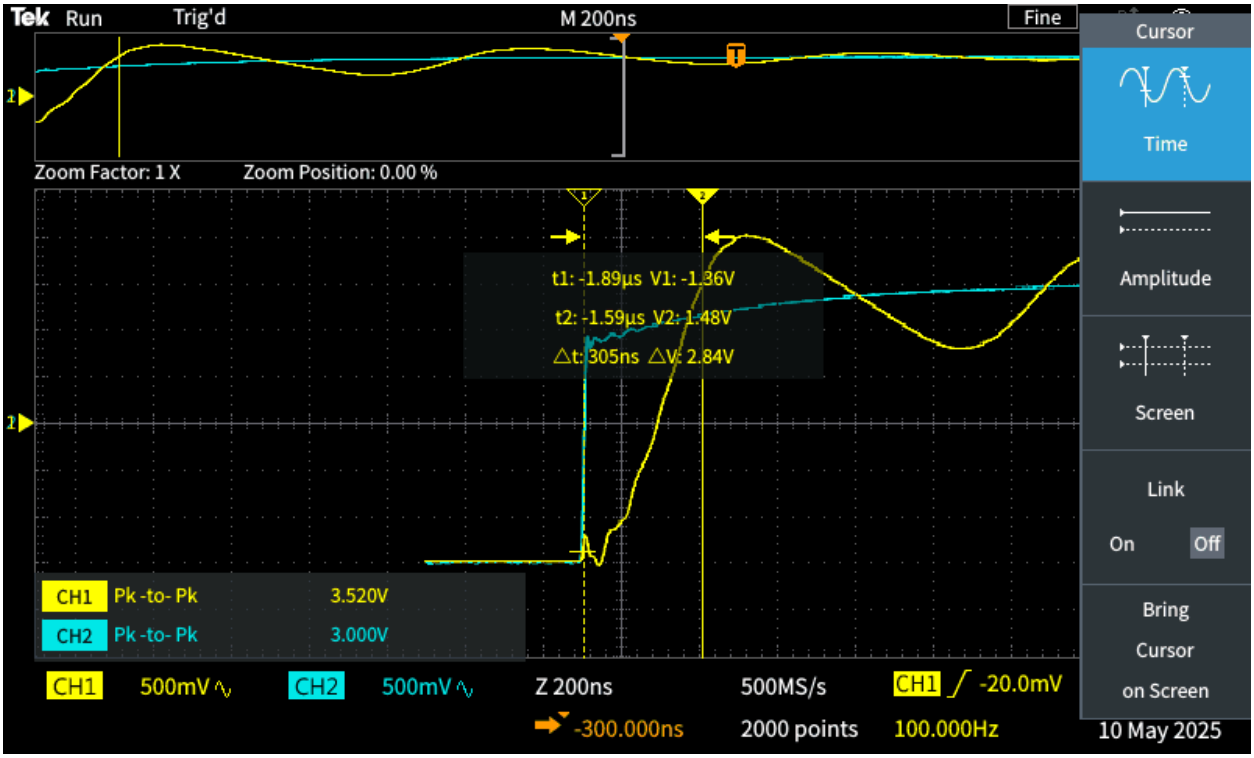
For part 2.6, it was asked to measure the time it takes for the output to reach 95% of its final value or when the output stabilizes, the measurement needed to be estimated by the eye since it is hard to determine the 95% mark. The following scope shot displays the time it takes for the output to reach 95% of its final value which was measured to be 4.4 µs:



Scope Shot 4 - Time it Takes for the Output to Reach 95% of its Final Value

For part 2.7, it was asked to measure the rising and falling edge slew rates and include scope shots. The way the rising edge slew rate was measured using the oscilloscopes time cursors to determine the 10 % and 90% mark of its total rise time and divide the difference in voltage by the difference in rise time from 10% to 90% which the calculation is shown below along with the scope shot of the rising edge slew rate:

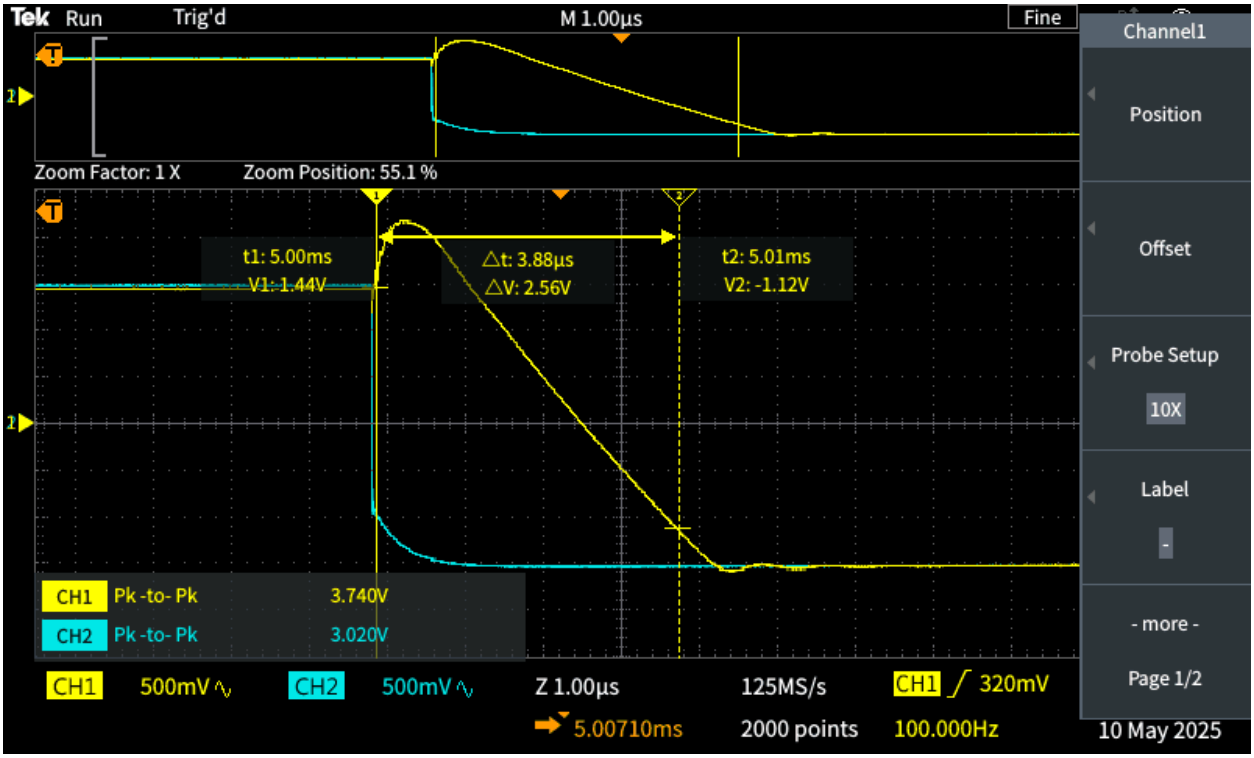
$$Rising\ Edge\ Slew\ Rate = \frac{\Delta V}{\Delta Tr} = \frac{2.84V}{305ns} = 9.31\frac{V}{\mu s}$$



Scope Shot 5 - Rising Edge Slew Rate

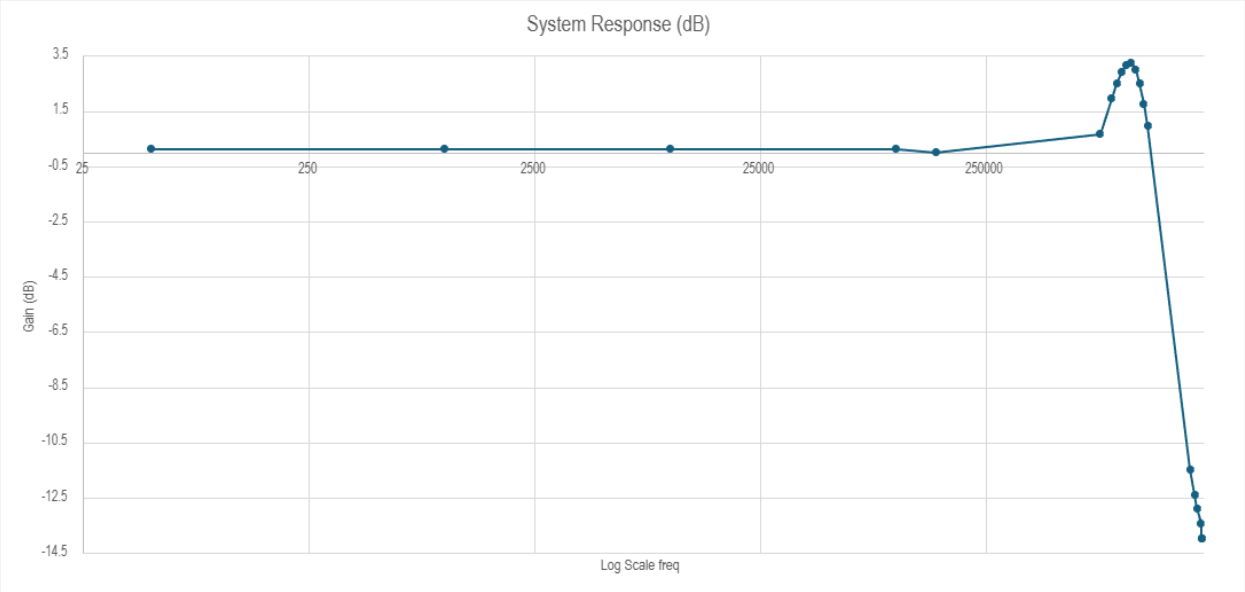
The same procedure was performed to measure the falling edge slew rate which would be by dividing the difference in voltage by the difference in time using the time cursors on the oscilloscope at the 90% and 10% points when the edge is falling which the calculation is shown below along with the scope shot of the falling edge slew rate:

$$Falling\ Edge\ Slew\ Rate = \frac{\Delta V}{\Delta Tf} = \frac{2.56V}{3.88\mu s} = 0.660\frac{V}{\mu s}$$



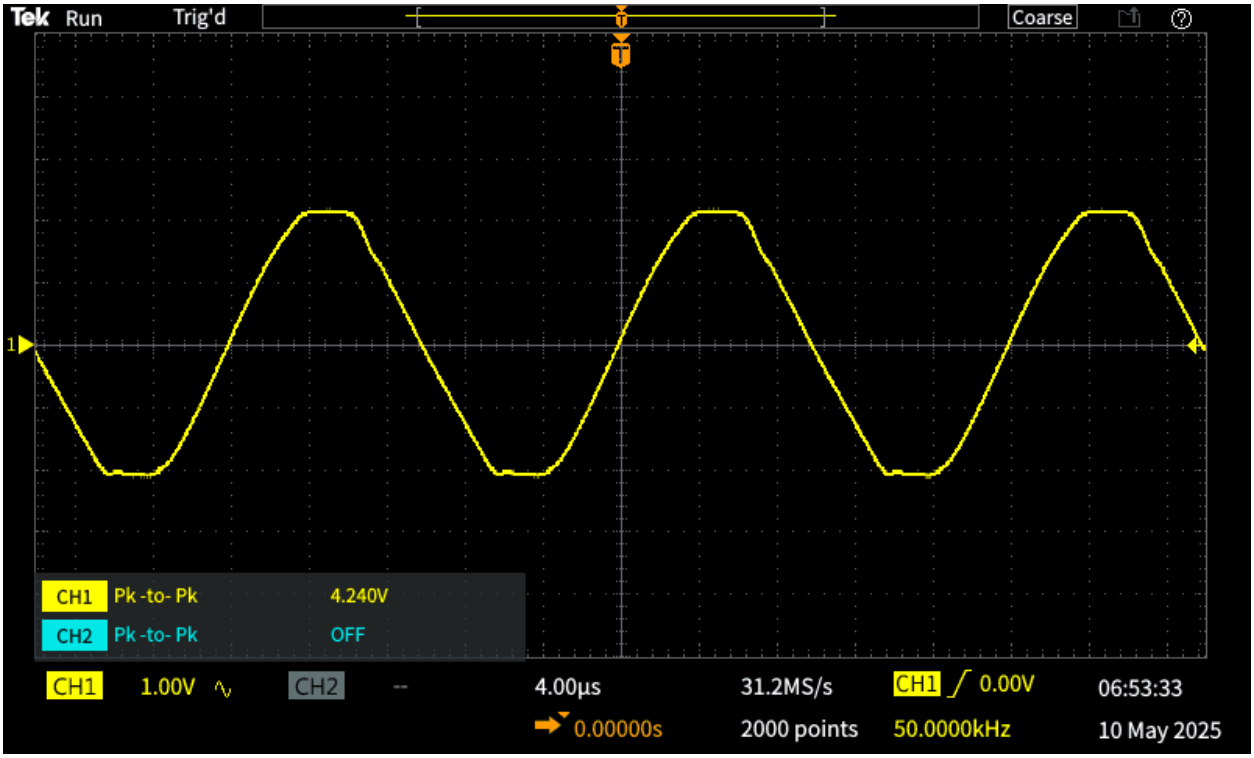
Scope Shot 6 - Falling Edge Slew Rate

For part 2.8, it was instructed to change the input waveform to a sine wave with a very small amplitude and measure the frequency response of the circuit. The following graph displays the frequency response of the circuit by varying the frequency and getting the gain at various points:



Bode Plot 1 - Frequency Response of the Voltage Follower Circuit in dB

For part 2.9, it was asked to pick a frequency within the passband and raise the amplitude of the sine wave until the output starts to get clipped, the voltage at the clipping point is the output's voltage swing. The measured output voltage swing displayed on the oscilloscope showed a voltage of 4.24V peak-to-peak which the scope shot will be displayed below:



Scope Shot 7 - Clipped Sine Wave Output Displaying Voltage Swing

The frequency high (fH) was measured by first, getting the 3 dB down point, since it's a voltage follower, the gain is 1 V/V; therefore, the 3 dB down point in decimal would be to divide the gain by square root of two which ends up giving 3 dB = 1/sqrt(s) = 0.707VV. That voltage of 0.707 V/V is the gain at which the 3 dB down point is located, in other words, the frequency will be swept until the gain reaches ~0.707 V/V. After sweeping the frequency, it was observed that the 3 dB down point for fH happens at 1.64 MHz, so the frequency high fH = 1.64 MHz. Next, the Gain Bandwidth (GBW) was calculated which the following equation shows the gain bandwidth of the circuit:

$$GBW = fH * Av = (1.64\ MHz)\left(1\frac{V}{V}\right) = 1.64\ MHz$$

III. SUMMARY OF RESULTS

Parameter	Result
Current Source (Calculated)	75 µA
Current Source (Measured)	~70.1 µA
Initial Power Dissipation	0.3893 mW
Step Response Settling Time	4.4 µs
Rising Edge Slew Rate	9.31 V/µs
Falling Edge Slew Rate	0.660 V/µs
Frequency Response (fH)	1.64 MHz
Gain Bandwidth Product (GBW)	1.64 MHz
Output Voltage Swing	4.24 V peak-to-peak

IV. CONCLUSION

The experiment involved designing, constructing, and testing a two-stage CMOS Op Amp to validate its open-loop and closed-loop performance. Initial tests confirmed proper biasing, with a measured power dissipation of 0.3893 mW, indicating efficient transistor operation in saturation. Open-loop testing demonstrated the Op Amp's comparator behavior, producing square-wave outputs when driven by a 1.5 V amplitude sine wave.

Compensation using a 100 pF capacitor and adjustable resistor optimized the step response, achieving a settling time of 4.4 μs to 95% of the final value. The disparity between rising (9.31 V/μs) and falling (0.660 V/μs) slew rates highlighted asymmetries in the output stage's current sourcing and sinking capabilities. Frequency response analysis revealed a 3 dB bandwidth of 1.64 MHz, aligning with the gain-bandwidth product (GBW) of 1.64 MHz, consistent with unity-gain stability. The output voltage swing of 4.24 V peak-to-peak confirmed near-rail-to-rail performance under clipping conditions.

This lab underscored the importance of compensation in stabilizing feedback systems and the practical challenges of component matching in discrete Op Amp designs. Key learnings included the impact of parasitic capacitances on transient response, the trade-offs between slew rate and bandwidth, and the necessity of iterative tuning in analog circuit design. These insights bridge theoretical models with real-world implementations, emphasizing precision in measurement and adaptability in troubleshooting.

University of Texas – Rio Grande Valley

EECE 3225 / EECE 3230

LAB DEMONSTRATION CERTIFICATION

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This section to be filled in by project team

Course EECE 3302 Project Electronics 2 project

Team Members :

1. Emilio
2. Jordan
3. _____

Describe what is being demonstrated:

Voltage Follower config.

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This section to be filled in by instructor

Signature: _____ Date: May 14 2025 Time: 1:44 pm

Comments:

CRWS

Op-Amp

If an instructor is not available at demo time, this form can be signed by an EE faculty, teaching assistant, or lab technician. Tape or paste this certification in the lab notebook.